

REMARKS

After the foregoing Amendment, Claims 32, 34-36, and 38-39 are currently pending in this application. Claims 4, 11, 14-17, 21 and 24 have been withdrawn for prosecution as being directed to non-elected subject matter. Claims 1-3, 5-10, 12-13, 18-20, 22-23, 25-31, 33, and 37 have been canceled without prejudice. Claims 32 and 34-36 have been amended to expedite the prosecution of the present application. New claims 38-39 have been added to more distinctly claim subject matter which the Applicants regard as the invention. Applicants submit that no new matter has been introduced into the application by these amendments.

The specification has been amended to conform the text to the figures.

Applicants wish to thank Examiner Nguyen for the courtesy of granting a telephone interview and further wishes to thank the Examiner for the suggestions put forth during the course of the interview in order to expedite the prosecution of the present application.

Claim Objections

The Examiner objected to claim 28 for lack of antecedent basis. Since claim 28 has been canceled, the objection of the claim is considered moot.

Claim Rejections - 35 USC § 112

Claims 33 and 34 stand rejected under 35 USC § 112, 2nd paragraph as being indefinite. Claim 33 has been cancelled without prejudice therefor making the rejection moot. Regarding claim 34, Examiner states that:

"None of the drawings show that the claimed circuit is a slew rate detector i.e., dv/dt detection. The circuits of the present application merely response to the level of the input signal during rising/falling time...The circuit only detects the level of the rising or falling input signal. It is inherent that when any input signal changes from low to high or high to low with a rate(slew rate dv/dt or -dv/dt)."

Figure 2a in fact shows that a tracking circuit can detect a change of an input signal from a positive slope, dv/dt, to a negative slope, -dv/dt. Moreover, Pg. 5, lines 18-20 states:

"Figure 2B shows slightly more detailed schematic as compared with Figure 2A, in which the **tracking system 10 is a dv/dt analyzer** operating a charge pump 11 to compensate for charging or discharging of parasitic capacitor C_p." (Emphasis Added)

The operation of the circuit under a rising edge scenario is described in Pg. 5, line 28 to Pg. 6, line 3 which states:

"In operation, **during a rising edge signal (+dv/dt)**, since the voltage of C_T cannot change instantaneously, the voltage increases at terminal 22 which ultimately causes the drain of PMOS transistor 20 to provide sufficient

current at terminal 24 to compensate for a portion of the current that would otherwise be provided to parasitic capacitance C_T by the input signal."
(Emphasis Added)

The operation of the circuit under a negative edge scenario is described in Pg. 6, lines 4-7 which states:

"During the **negative edge of the signal** ($-dv/dt$), the voltage instantaneously decreases at terminal 22 which ultimately causes the transistor 20 to prevent the voltage level of terminal 24 to be reduced, thereby preventing occurrence of a glitch during the negative going portion of the input signal." (Emphasis Added)

Therefor the present invention can do more than "merely response to the level of the input signal during rising/falling time...The circuit only detects the level of the rising or falling input signal." One way it can detect a rise or a fall in the input signal is by analyzing a change in dv/dt . Tracking the rate of increase or decrease of an input is different from merely detecting a rise or fall in level. For example, a large rate of increase, dv/dt , may let the correction circuit know that a large current will be needed for charging the parasitic capacitance. If the detector merely responded to a rise in the input signal, the correction circuit would have no information regarding the degree of the rise. Therefor, tracking dv/dt is more than an inherent feature of the present invention.

Claim Rejections - 35 USC § 102(b) Bruccoleri et al.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25, and 28-36 stand rejected under 35 USC § 102(b) as being anticipated by Bruccoleri et al.(US Pat. 5,808,488). Claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25, 28-31, and 33 have been canceled without prejudice, therefore making the rejection moot. Regarding Claims 32 and 34 have been amended in order to make the Claims allowable over Bruccoleri et al. No where does Bruccoleri et al. state the use of a charge pump for compensating for a parasitic capacitance during a change of the input signal to a circuit. Bruccoleri et al's invention is "to provide a timed bistable circuit (latch) having a reduced offset which is substantially independent of the timing frequency." Column 1, lines 63-65) Bruccoleri et al does not disclose a means for compensating for parasitic capacitances to an input of a circuit.

Claims 35, 36, 38, and 39 are dependent upon claim 34, which the Applicants believe are allowable over the cited prior art of record for the same reasons provided above.

Based on the arguments presented above, withdrawal of the 102(b) rejection of claims 32, 34-36 is respectfully requested.

Applicant: Drapkin et al.
Application No.: 09/651,944

Claim Rejections - 35 USC § 102(b) Hemdal et al.

Claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25, and 28-31 stand rejected under 35 USC § 102(b) as being anticipated by Hemdal et al.(US Pat. 5,999,042). Claims 1-3, 5, 6, 8, 9, 12, 13, 18, 25, and 28-31 have been canceled without prejudice, therefor making the rejection moot.

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Conclusion

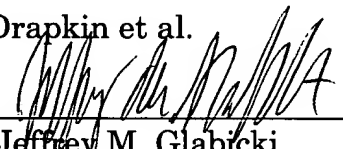
If the Examiner believes that any additional minor formal matters need to be addressed in order to place this application in condition for allowance, or that a telephone interview will help to materially advance the prosecution of this application, the Examiner is invited to contact the undersigned by telephone at the Examiner's convenience.

Reconsideration and entry of this amendment is respectfully requested.

Respectfully submitted,

Drapkin et al.

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